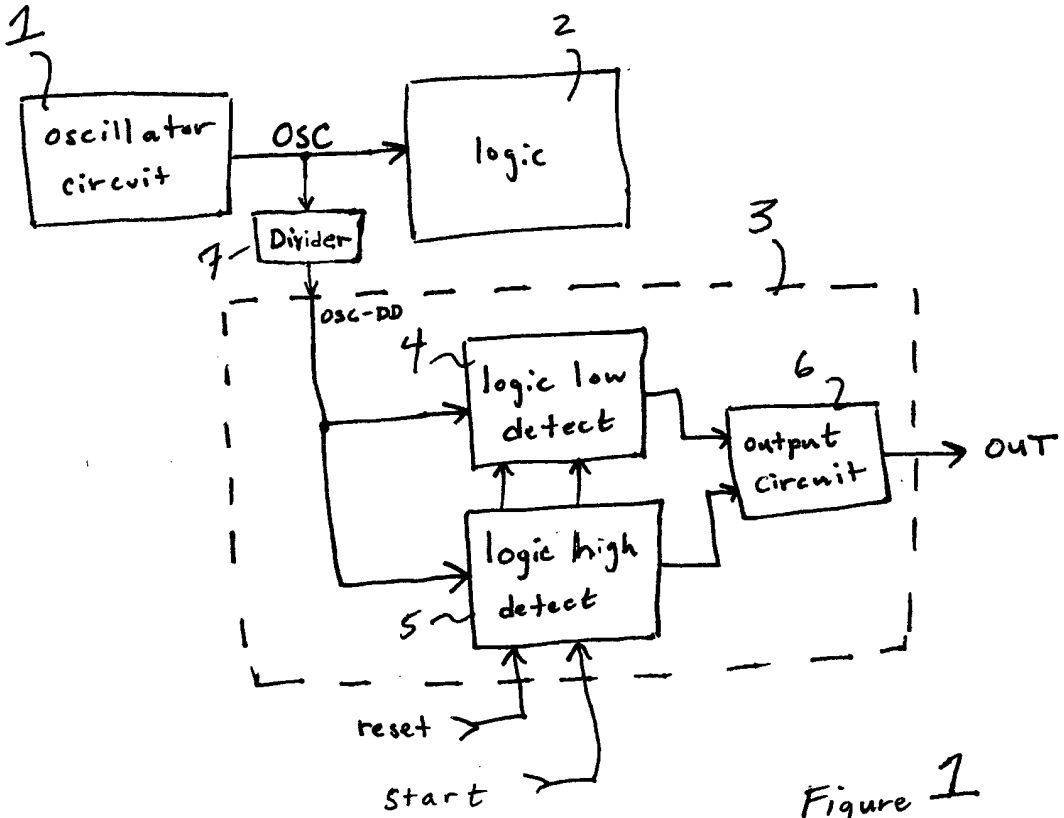
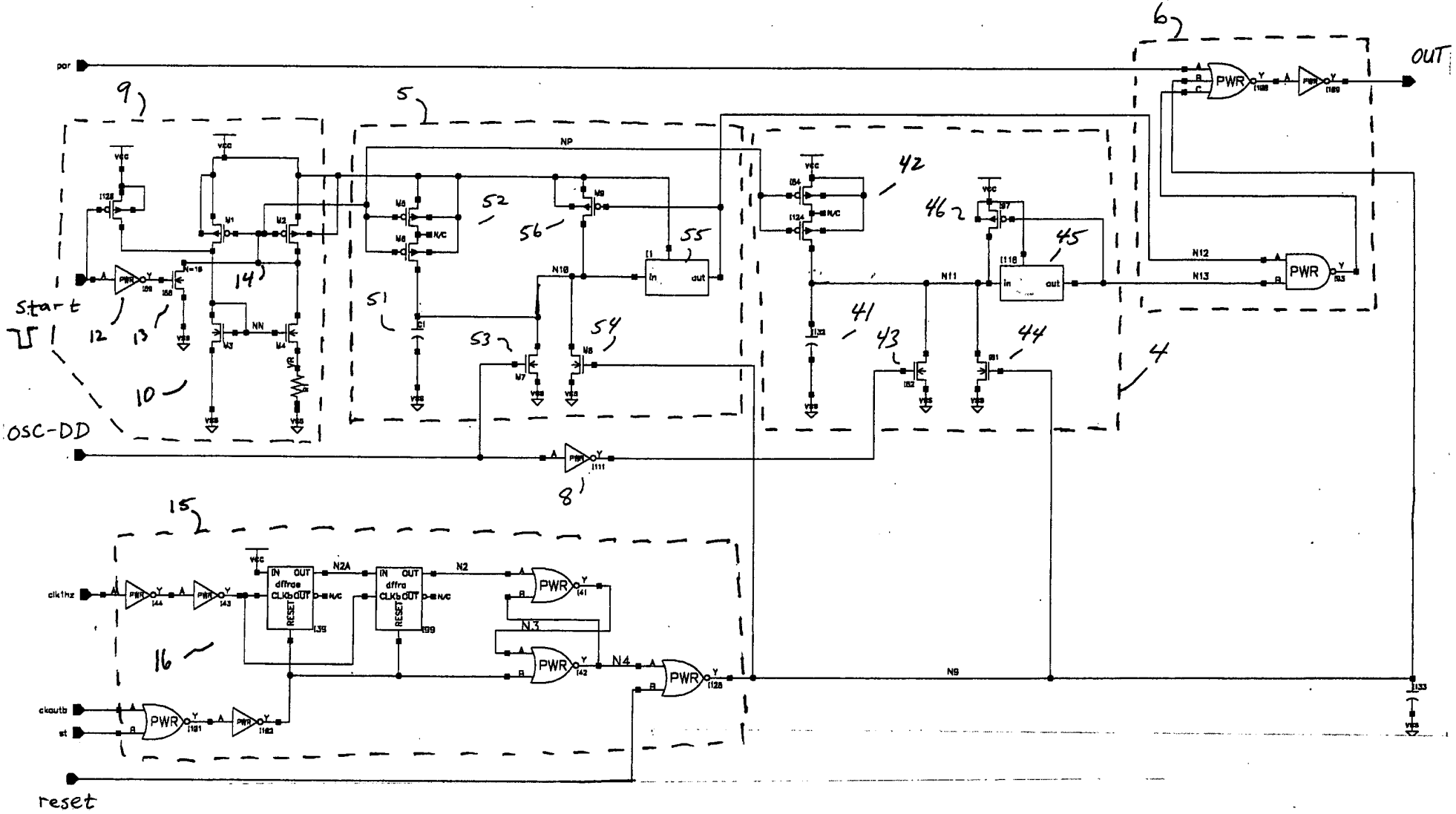

1
oscillator circuit
OSC
2
logic
Divider
7
3
OSC-DD
4
logic low detect
6
output circuit
OUT
logic high detect
5
reset
Start

Figure 1


por
OUT
start
OSC-DD
reset
clk1hz
ckoutb
st
PWR
Vcc
Vss
NP
N11
N12
N13
N18
N2
N2A
N3
N4
N8
NN
RESET
9
5
6
4
10
12
13
14
15
16
8
41
42
43
44
45
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51
52
53
54
55
56

Figure 2

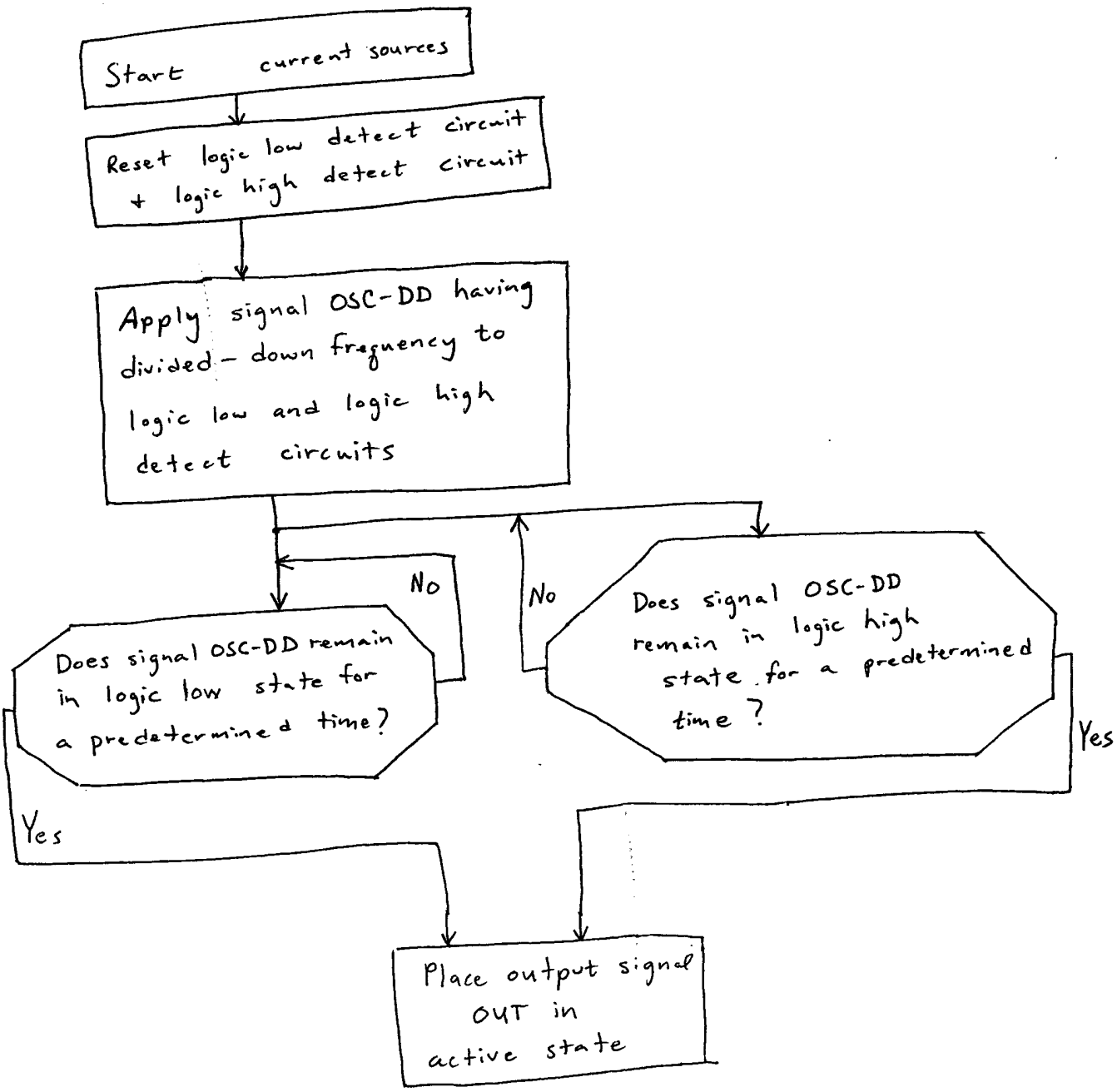
Start current sources
Reset logic low detect circuit + logic high detect circuit
Apply signal OSC-DD having divided-down frequency to logic low and logic high detect circuits
Does signal OSC-DD remain in logic low state for a predetermined time?
No
Yes
Does signal OSC-DD remain in logic high state for a predetermined time?
No
Yes
Place output signal OUT in active state

Figure 3